Voltage Level Shifter Using Modified Wilson Current Mirror

N. Minakhi, Priyanka Karmakar

Abstract-A Low Power Voltage Level Shifter is used as an intermediate between blocks and systems. This Voltage Level Shifter uses low-power to convert sub-threshold voltage level to above threshold voltage levels. This paper presents a Voltage Level Shifter which has an operating range from sub-threshold level to supply voltage. The Proposed Voltage Level Shifter uses a Modified Wilson Current Mirror and an Inverter.The circuit is able to convert a wide range of voltage levels to other levels. The circuit is designed in 180nm, 90nm and 45nm CMOS Technology in Cadence Virtuoso Simulator and simulation is done.The parameters such as power, delay, PDP and area is calculated. Propagation delay is decreased by 10% and power consumption by 12%.

Keywords- Current mirror, DELAY, PDP, Power Consumption, Power Dissipation**,** sub-threshold, Voltage level shifter,

I. INTRODUCTION

Now-a-days, everyone wants a device which is easy to handle, have smaller size, uses low- power and speed is more. The factors which are mainly focused in designing a circuit are TAP (Time, Area and Power).

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It means a device should be have smaller area, uses low power and should produce output in time with less power dissipation and less propagation delay [9].During manufacturing of a device these factors are considered mainly. Area can be reduced by shrinking the size of transistors used in the circuit. And, power dissipation can be reduced by decreasing the supply voltage because power dissipation is square of power supply [1-2], [10]. So, by reducing supply power, propagation delay increases in the circuit which is a major disadvantage.[1]

In larger circuits, the whole circuit is divided into smaller parts and each part is assigned with individual supply [1-3]. Supply voltage can be applied to different blocks on the basis of output generation in the circuit. For example, if the output of a block in the circuit is time-critical means the block has to provide an output on time where no delay in output is considered those circuits are applied with high supply voltage and, parts of a circuit where delay in output can be accepted are applied with low supply. But, disadvantage is that the higher voltage parts sometimes does not identify changes due to low voltage parts. [2] Hence, Voltage Level Shifter is used. It plays a key role between blocks using different power supply for their operation.

Here, a Voltage Level Shifter is proposed which has less area, less delay and power dissipation is less.

In the design of the proposed Voltage Level Shifter a Modified Wilson Current Mirror is used [1].

Current Mirror is a circuit which copies the current from the original active device to the other device.

II. CONVENTIONAL VOLTAGE LEVEL SHIFTER [1]

In order to have a comparison between different Level Shifters and proposed Level Shifter.

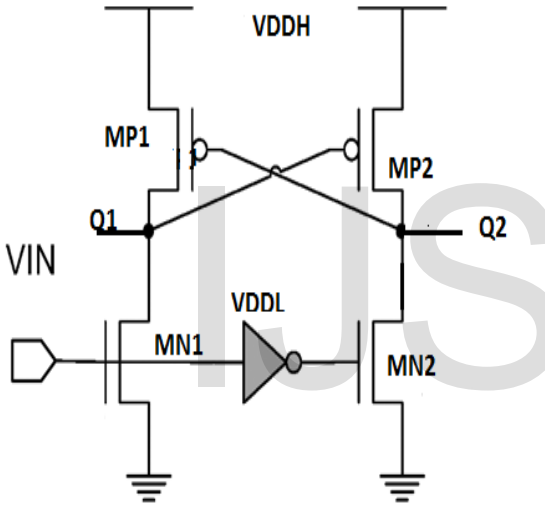


Fig.1 Schematic of Conventional Voltage Level Shifter [1]

When input signal is high, NMOS MN1 is on, making MN2 off. Node Q2 is pulled up to VDDH making MP2 and MP1 on and off respectively and node Q1 is pulled down. When input signal is low, NMOS MN1 and MN2 are off and on respectively. Then node Q1 is pulled up to VDDH making MP1 and MP2 ON and off respectively and Q2 is pulled down.

The major disadvantage is that there is a contention between NMOS and PMOS when NMOS tries to pull down the output node . To eradicate this problem, NMOS transistor size needs to be increased which further increases delay in the circuit.

To solve the problem of contention between NMOS and PMOS which a raised in Conventional Voltage Level Shifter, Voltage Level Shifter using Modified Wilson Current Mirror with Hybrid Buffer is used. [2]

The whole circuit is further divided into three blocks- one blocks comprises of a Modified Wilson Current Mirror, second is the delay path and third one is the complementary OR gate. [1]

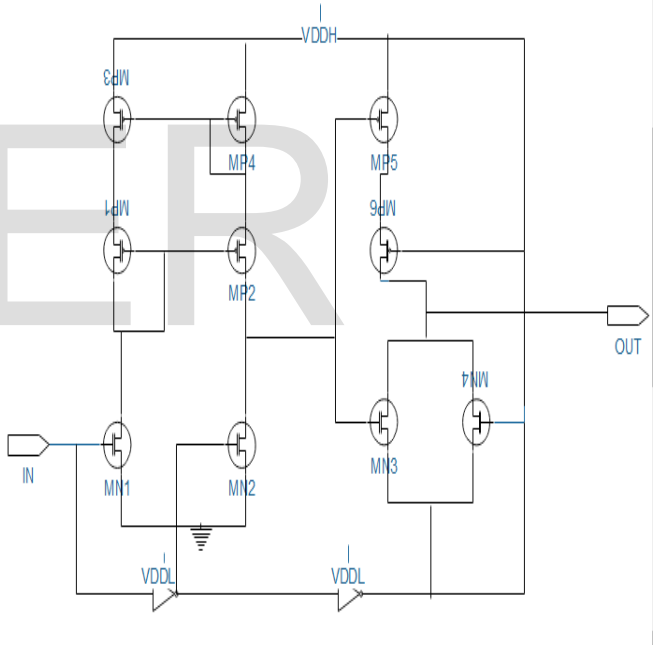


Fig.2 Schematic of Level Shifter using Modified Wilson Current Mirror Hybrid Buffer [2]

The operation of this Voltage Level Shifter is as follows, when input signal to the Level Shifter is high, MN1 and MN2 are on and off respectively. PMOS MP1 and MP2 are off and on respectively and the output of the Current Mirror is high. This output is fed to the Complementary OR

gate and at node B the output is also high. So, MP5 is off and MP6 is also off giving output as high signal. The output of Complementary OR gate is fed to Inverter and we get high output from the inverter.

When input signal is low, MN1 is off and MN2 is on. And PMOS MP1 is on and MP2 is off and the output of Current Mirror is low. This output is fed to the Complementary OR gate and at node B the output is low. So, MP5 and MP6 are in on state making the output of Complementary OR as high. This output is given to the inverter and we get a low output signal from the inverter.

III. PROPOSED STRUCTURE

The above structure is a Level Shifter having Modified Wilson Current Mirror, complementary OR gate and an inverter in the output side acts as a Level Shifter when difference between two voltages are small. To reduce power consumption complementary OR gate and inverter from the output side are removed. The proposed structure uses a Modified Wilson Current Mirror and an inverter between two NMOS. Since, the OR gate and inverter parts are removed the circuit becomes small. The operation is as follows, when input is high, MN1 and MN2 are on and off respectively. MP1 goes off and MP2 is on and output is taken as high. When input is low, MN1 is off and MN2 goes on making MP1 and MP2 on and off respectively.

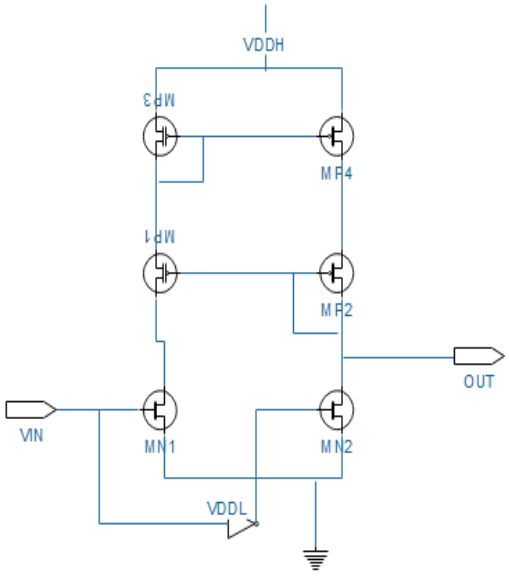


Fig.3 Schematic of Proposed Level Shifter

IV.SIMULATION RESULTS

The Proposed Level Shifter is simulated in different technologies, 180nm, 90nm and 45nm in Cadence Virtuoso Simulator in order to verify the performance in different technologies. Different types of level Shifters are also simulated keeping all the circuit parameters same as the parameters of the proposed circuit to have a fair comparison. Delay, power consumption and area of the circuits are compared.

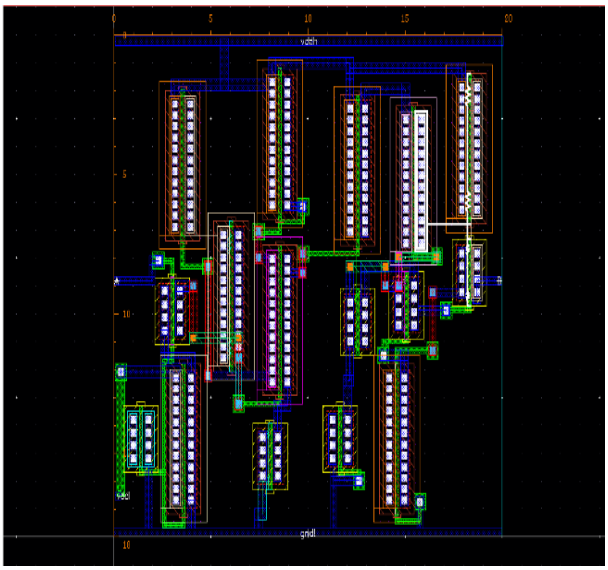
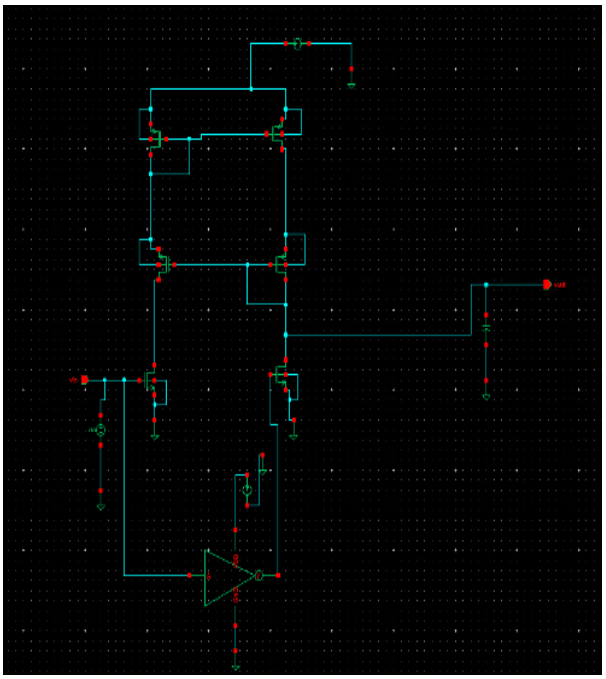
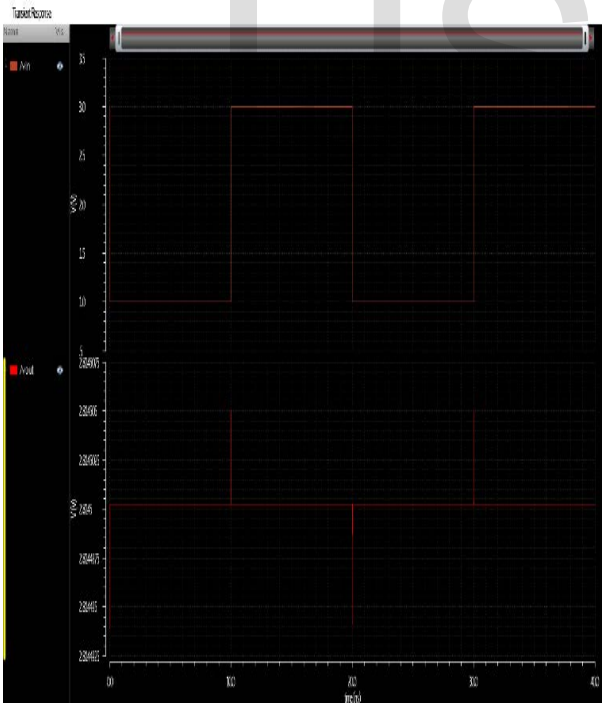


Fig.4 Layout of Level Shifter using Modified Wilson Current Mirror Hybrid Buffer [2]



(a)



(b)

Fig.5 (a) Schematic of Proposed Level Shifter

(b) Simulated Waveform

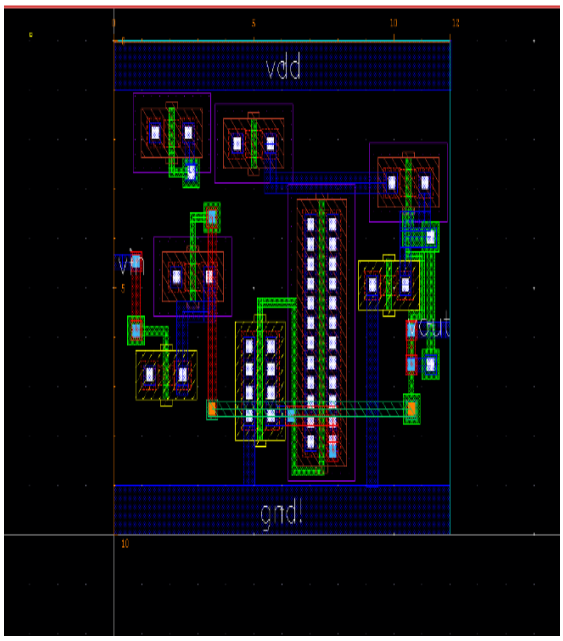


Fig.6 Layout of the Proposed Level Shifter

The power supply is changed to view the difference in power consumption. When VDH=3V and VDDL=1V is chosen , then VDDH=1V and VDDL=0.2V is applied and the delay and power consumption are compared.

TABLE-1

COMPARATIONOF PROPAGATION DELAY IN DIFFERENT TECHNOLOGIES

With VDDH=3V, VDDL=1V

TYPES OF LEVEL SHIFTERS	**180nm (in sec)**	**90nm (in sec)**	**45nm (in sec)**
CONVENTIONAL LEVEL SHIFTER	$5.29 * 10^{-9}$	$1.56 * 10^{-11}$	$4.78 * 10^{-12}$
LEVEL SHIFTER USING MODIFIED WILSON CURRENT MIRROR HYBRID BUFFER	$3.22 * 10^{-9}$	$1.37 * 10^{-11}$	$1.132 * 10^{-11}$
PROPOSED LEVEL SHIFTER	$1.56 * 10^{-9}$	$5.68 * 10^{-12}$	$4.49 * 10^{-12}$

TABLE-2

COMPARATION OF POWER CONSUMPTION IN DIFFERENT TECHNOLOGIES

With VDDH=3V, VDDL=1V

TYPES OF LEVEL SHIFTERS	180nm (in Watts)	90nm (in Watts)	45(in Watts)
CONVENTIONAL LEVEL SHIFTER	202* 10^{-9}	148* 10^{-9}	107* 10^{-9}
LEVEL SHIFTER USING MODIFIED WILSON CURRENT MIRROR HYBRID BUFFER	529.2 *10^{-6}	340.9* 10^{-6}	246* 10^{-9}
PROPOSED LEVEL SHIFTER	188.3 *10^{-9}	168* 10^{-9}	142* 10^{-9}

TABLE- 3

COMPARATIVE TABLE SHOWING PDP OF LEVEL SHIFTERS IN DIFFERENT TECHNOLOGIES

With VDDH=3V, VDDL=1V

TYPES OF LEVEL SHIFTERS	180nm (in Joules)	90nm (in Joules)	45nm(in Joules)
CONVENTIONAL LEVEL SHIFTER	1.06* 10^{-15}	2.30* 10^{-18}	5.10* 10^{-19}
LEVEL SHIFTER USING MODIFIED WILSON CURRENT MIRROR HYBRID BUFFER	1.70* 10^{-12}	4.67* 10^{-15}	2.79* 10^{-18}
PROPOSED LEVEL SHIFTER	2.93* 10^{-16}	9.54* 10^{-19}	6.37* 10^{-19}

TABLE-4

COMPARATIONOF POWER CONSUMPTION IN DIFFERENT TECHNOLOGIES

With VDDH=1V, VDDL=0.2V

TYPES OF LEVEL SHIFTERS	180nm (in Watts)	90nm (in Watts)	45nm (in Watts)
CONVENTIONAL LEVEL SHIFTER	178.8 *10^{-9}	143.4 *10^{-9}	103.6* 10^{-9}
LEVEL SHIFTER USING MODIFIED WILSON CURRENT MIRROR HYBRID BUFFER	488* 10^{-6}	332* 10^{-6}	192* 10^{-9}
PROPOSED LEVEL SHIFTER	145.9 *10^{-9}	126.7 *10^{-9}	102.2* 10^{-9}

TABLE-5

COMPARATIONOF PROPAGATION DELAY IN DIFFERENT TECHNOLOGIES

With VDDH=1V, VDDL=0.2V

TYPES OF LEVEL SHIFTERS	180nm (in seconds)	90nm (in seconds)	45nm(in seconds)
CONVENTIONAL LEVEL SHIFTER	9.68* 10^{-9}	4.56 *10^{-11}	2.30* 10^{-11}
LEVEL SHIFTER USING MODIFIED WILSON CURRENT MIRROR HYBRID BUFFER	8.80 *10^{-9}	5.67* 10 $^{-11}$	3.70* 10^{-11}
PROPOSED LEVEL SHIFTER	3.23 *10^{-9}	1.20* 10^{-11}	5.79* 10^{-11}

TABLE-6

COMPARATION OF PDP IN DIFFERENT TECHNOLOGIES

With VDDH=1V, VDDL=0.2V

TYPES OF LEVEL SHIFTERS	**180nm (in Joules)**	**90nm (in Joules)**	**45nm(in Joules)**
CONVENTIONAL LEVEL SHIFTER	$1.73*10^{-15}$	$6.53*10^{-16}$	$2.38*10^{-17}$
LEVEL SHIFTER USING MODIFIED WILSON CURRENT MIRROR HYBRID BUFFER	$4.29*10^{-11}$	$1.88*10^{-14}$	$7.10*10^{-18}$
PROPOSED LEVEL SHIFTER	$4.71*10^{-16}$	$1.52*10^{-19}$	$5.91*10^{-18}$

TABLE-7

COMPARATION OF AREA OF LEVEL SHIFTERS USING LAYOUT IN DIFFERENT TECHNOLOGIES

TYPES OF LEVEL SHIFTERS	**180nm**	**90nm**	**45nm**
LEVEL SHIFTER USING MODIFIED WILSON CURRENT MIRROR HYBRID BUFFER	$300um^2$	$120um^2$	$45um^2$
PROPOSED LEVEL SHIFTER	$120um^2$	$20um^2$	$9um^2$

Table1,2 and 3 summarizes delay, power consumption and PDP of different level shifters at different technologies when VDDH=3V and VDDL=1V. Table 4,5 and 6 shows delay, power consumption and PDP of different level shifters at different technologies when VDDH=1V and VDDL=0.2V. And, Table 7 shows area of level shifters at different technologies.

V. CONCLUSION

The above schematics are simulated in Cadence Virtuoso simulated at 180nm, 90nm and 45nm CMOS technology. The propagation delay, power consumption and PDP are verified. For VDDH=1v and VDDL=0.2v, the delay is reduced by 10%, power consumption is decreased by 12% in 45nm technology.

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